Probing Transistors at the Contact Level in Integrated Circuits

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Introduction

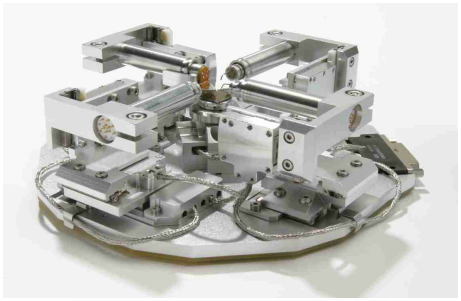
Probing integrated circuits (IC) with sharp metal contact wires under an optical microscope has been, for many years, the primary means of characterizing an IC's electrical performance. Since advances in IC technology follow Moore's Law of decreasing scale, the complexity of producing and testing the more advanced IC's has increased. More powerful microscopes and highly precise probe placement is needed in order to test these next-generation ICs.

Scanning electron microscopes (SEMs) and focused ion beam (FIBs) systems are widely employed to image and measure the results of different IC fabrication steps. SEMs and FIBs are ubiquitous to most fabs and are workhorse instruments for metrology and failure analysis. The Zyvex KZ100 prober, which is compatible with both system platforms, greatly enhances the utility of these common tools by enabling IC electrical performance measurements at the nano scale.

Extrapolating data from test devices in the scribe line (street) is a common method of testing. However, scribe line devices are known to behave differently than devices in the real application. Alternatively, test modules can be designed and placed on-chip, but this technique requires valuable real estate. Probing in die transistors, that are actual devices, at the contact level has proven to be an invaluable technique. With data collected from individual on-chip transistors using the KZ100, IC design engineers can feed actual device data into design models to improve modeling accuracy.

The Zyvex KZ100 Nanomanipulator/Prober is comprised of a Zyvex Nanomanipulator **(Figure 1A)**, controller **(Figure 1B)** and a Keithley 4200 Semiconductor Characterization System **(Figure 1C)**. The KZ100 is capable of landing four sharp probes easily within a 200 x 200 nm area with less than 5 nm precision. The size of the minimum landing area is dependent on the sharpness of the probes. With FIB sharpened probes, the minimum landing area could be much smaller than that stated above. The KZ100's range of motion and precision makes the KZ100 ideal for probing ICs that are fabricated with 90 nm node technology. As IC technology advances and the scale decreases, to 60 and then to 45 nm, the

(a)



(b)

(c)

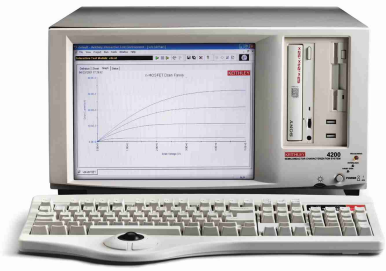


Figure 1
(a) KZ100 head unit with end-effectors installed.
(b) Zyvex KZ100 Controller.
(c) Keithley 4200 Semiconductor Characterization System.

KZ100 is also well-positioned to probe next generation ICs. An SEM/FIB is typically optimized for low mechanical and electrical noise, which is necessary to achieve sub-nanometer resolution images. Ambient conditions which commonly affect AFM systems, such as thermal fluctuations and air drafts, are thus eliminated by the controlled environment of the SEM or FIB.

Systems that rely on atomic force microscopy (AFM) techniques in air can require extensive and expensive facilities upgrades. Requirements can typically include a mechanically quiet room, stabilized air flow conditions, and air temperature stability that can exceed many standard clean room HVAC specifications.

In addition, AFM scanning speeds are slow and fields of view are very limited resulting in very long and tedious exercises to locate a small specific region of interest. SEMs and FIB's offer the user the ability to image large areas quickly to find a region, and then magnify specific portions to highlight particular areas. The KZ100 system benefits from utilizing the optimized vacuum chamber environment where high-resolution images of the IC test site can be generated with low electrical and mechanical noise, probe placement can be directed without ambient interferences, and external influences on probe drift are minimized.

Application

The KZ100 can be outfitted with as many as four probes which are independently and linearly operated in X, Y, and Z with less than 5 nm precision. For the purposes of this paper, the KZ100 was installed in a high-resolution SEM for precise imaging and probe placement similar to the arrangement shown in **Figure 2**. Tungsten probes with a 45-degree bend were prepared using a proprietary Zyvex process and installed in the four positioners. The 90 nm node IC test chip was deprocessed to the contact level and etched for five seconds in 20 parts H_2O to 1 part 49% HF. The IC chip was mounted to the grounded center rotational stage of the KZ100.

After SEM pump down and the microscope image parameters were determined, the IC test area was located and the probes were positioned above the test area. The probes were moved towards the IC surface and probe-to-surface contact was established. Once the probes were in contact with the IC, the probes were lifted just above the surface and then moved parallel to the surface until each probe was relocated above its intended circuit contact.

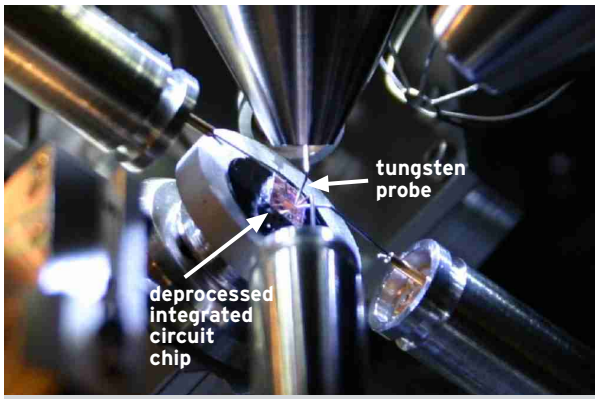


Figure 2 KZ100 Manipulator in an FIB at 52 degree tilt. The sample being probed on the center stage is a deprocessed integrated circuit chip.

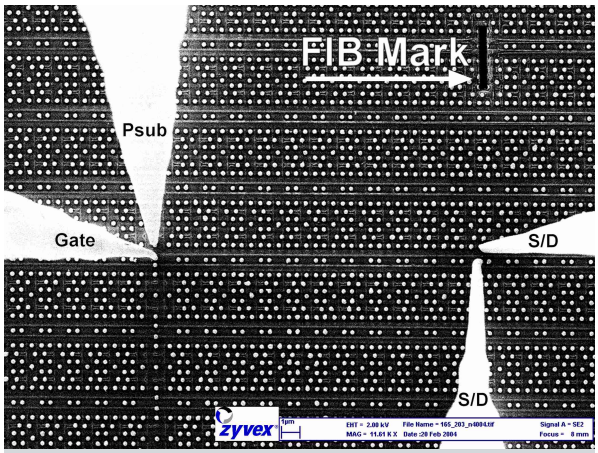


Figure 3 Four probe contact on an n-channel MOSFET. The Gate probe is connected to the pass-gate shared by four n-channel transistors. The Psub probe is connected to the substrate contact and the S/D probes are connected to the source and drain of the transistor being tested. The KZ100 is capable of connecting to contacts that are separated by as little as 70 nm and as large as 10 millimeters.

While the probe was re-lowered to the circuit contact, the probe was swept back and forth to determine contact and its location. Once the probe made contact, the probe's sweeping motion became a pivoting motion with the pivot point at the location where the probe touched the IC surface. The probe was then positioned so that the pivot point was coincident with the IC device contact. **Figure 3** shows four probes in electrical contact with the drain, source, gate and P substrate contacts of an n-channel MOSFET device.

A Keithley 4200 Semiconductor Characterization System was used for biasing the probes and collecting the IC device drain current vs. drain source voltage (I_DV_{DS}) data. The system was equipped with four 4200-SMUs (source measurement unit) and triaxial cabling. The I_DV_{DS} curves were acquired with the mode set to "sweeping" and the speed setting of "fast." The current compliance for the source and drain current I_S and I_D respectively was set to 500 µA and the voltage V_{DS} was swept with steps of 5 mV from 0.0 V to 1.5 V. A series of I_DV_{DS} curves were measured by additionally stepping the gate voltage V_{GS} with limits of 1.5 V and 100 nA. Before and during data acquisition, the microscope's scanning beam was blanked to minimize any charge-induced influence.

Results and Discussion

MOSFETs behave like transconductance devices over most of their operational range where I_D is nearly constant for a given V_{GS}. This operational range is commonly referred to as the "saturation region." At small drain source voltage V_{DS}, MOSFET devices behave like a resistor where the drain current I_D is linearly proportional to V_{DS} and this region is commonly referred to as the "linear region."

The I_DV_{DS} data, shown in **Figure 4**, collected from a 90 nm node n-channel MOSFET device using the KZ100 system has both the linear and saturation regions of a typical MOSFET. **Figure 4a** shows the drain current with forward bias and **Figure 4b** shows the same IC's drain current with reverse bias. This comparison is one way to determine if the device is functioning properly. The I_DV_{DS} curves of **4a** and **4b** are very similar which this shows that the current device under investigation is functioning as expected.

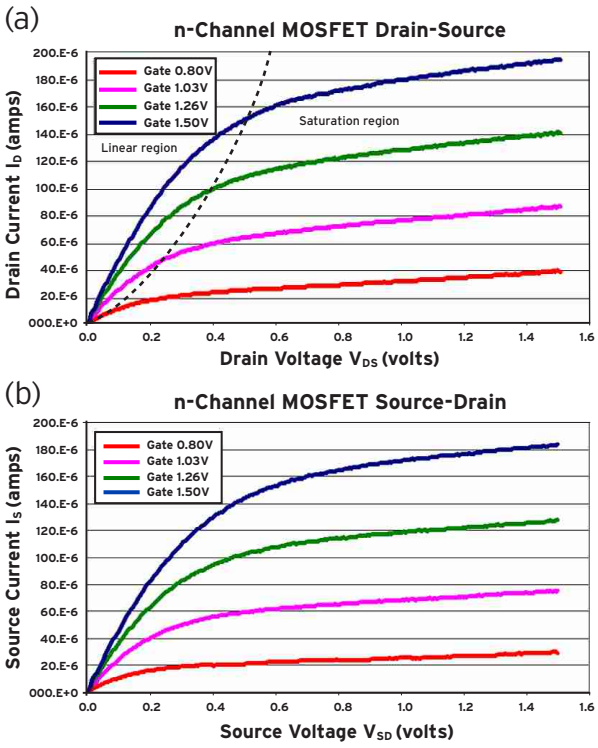


Figure 4
(a) The I_DV_{DS} curves of an integrated n-channel MOSFET generated by a Zyvex KZ100 Nanomanipulator System.
(b) The reverse bias of the device under test of Figure 4A.

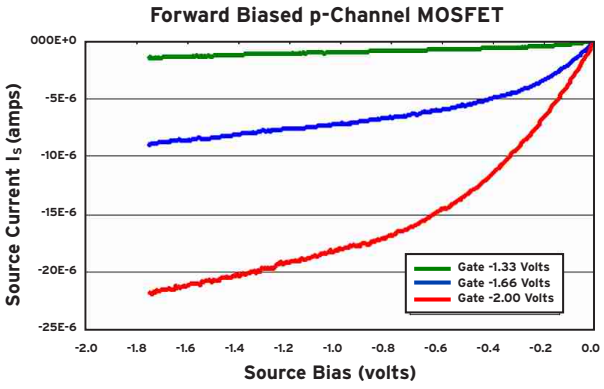


Figure 5 The I_SV_{SD} curves of an integrated p-type MOSFET generated by a Zyvex KZ100.

With p-channel MOSFETs, the current I_D flows when the gate voltage V_{GS} is negative with respect to the source voltage V_{DS}. Typically, p-channel MOSFETs have a higher gate threshold voltage and lower saturation current. **Figure 5** shows a family of I_DV_{DS} curves of a 90 nm node p-channel MOSFET device. These p-channel curves, collected using the KZ100, show the expected lower performance of a p-channel MOSFET in comparison with the n-channel MOSFET.

Conclusion

Electrical characterization of integrated circuits is an integral component of the fabrication and design loop. As high magnification scanning particle beam microscopes are needed to keep up with the decreasing scale of IC technology, electrical characterization using probing systems that are designed and optimized for operation in these microscopes is needed. The Zyvex KZ100 System is designed and optimized for characterizing current and next-generation IC device properties which require very precise probe placements, accurate current and voltage measurements, and high magnification inside a high resolution SEM or FIB system. With this system IC designers and failure analysis engineers are better equipped to tackle performance and failure issues of the next generation integrated circuits.